Claims 2-5, 10, 11, 17, 18, 22, and 23 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,369,437 B1 to MacPherson et al. Claim 2 recites a package including at least one pair of programmable elements. The Office Action refers to Fig. 1 of Macpherson, which teaches a conventional fuse array within an integrated circuit device. (Col. 4, lines 6-9). Because a package is distinct from an integrated circuit device, fuses in the device, taught by MacPherson, fail to teach the claimed package having a pair of programmable elements. Accordingly, Applicants respectfully submit that claim 2 and all claims dependent thereon are patentably distinguishable over MacPherson.

The Office Action responds to arguments previously presented by applicants by pointing out that MacPherson states (col. 1, lines 46, col. 2, line 32) that integrated circuit devices such as PALs, FPGAs, and PLDs are programmed as packaged units or after installation onto a circuit board. Therefore, the Office Action argues that Macpherson discloses an integrated circuit wherein the integrated circuit is part of a package and therefore it does not matter whether a package is distinct from a semiconductor. MacPherson teaches at col. 1, lines 46-51 that PALs, FPGAs, and PLDs are fabricated and programmed after they are packaged units. However, MacPherson distinguishes between a device and a package. For example, MacPherson teaches at col. 2, lines 5-7 that "the fuses in the device which define how the circuit is configured are accessed through the I/O pins on the device package." Applicants respectfully submit that it does matter whether a package is distinct from a semiconductor and respectfully request that the Examiner give appropriate consideration to that distinction.

As pointed our previously, Applicants distinguish between the device and the package. For example, the Applicants provide a definition in the specification at page 6, lines 2-10: "the term package as used herein is intended to include any integrated circuit carrier....In addition to the external connections, the package provides connections between chip 205 and package 207."

The meaning of the term "package" and its distinction from the device may also be obtained from a publicly available glossary. "Dictionaries, encyclopedias and treatises, publicly available at the time the patent is issued, are objective resources that serve as reliable sources of information on the established meanings that would have been attributed to the terms of the claims by those of skill in the art." *Texas Digital Sys., Inc. v. Telegenix Inc.*, 64 USPQ2d 1812,

1818 (Fed. Cir. 2002). In general, a package is "the protective container of an electronic component or chip. It includes the external terminals that provide electrical access to the components inside." LUCENT TECHNOLOGIES, GLOSSARY, *available at* http://www.lucent.com/search/glossary/glossary.html. Based on the aforementioned definitions, a package is distinct from a semiconductor device inside the package.

Similarly, claim 17 recites a package including one or more one-time programmable elements. Since MacPherson fails to teach a package having one-time programmable elements, as discussed above, Applicants submit that claim 17 and all claims dependent thereon are distinguishable over MacPherson.

The Examiner also suggests that the package limitation is not going to be given patentable weight because, where "the claim is drawing to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause (citing Kropa v. Robie, 88 USPQ 748 (CCPA 1951)).

Applicants respectfully disagree with the Examiner's application of case law and interpretation of the claims. "In general, a preamble limits the [claimed] invention if it recites essential structure or steps, or if it is 'necessary to give life, meaning, and vitality' to the claim." Pitney Bowes, Inc. v. Hewlett-Packard Co., 51 USPQ2d 1161, 1165 (Fed. Cir. 1999). "[A] claim preamble has the import that the claim as a whole suggests for it. In other words, when the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects." Bell Communications Research, Inc. v. Vitalink Communications Corp., 34 USPQ2d 1816, 1820 (Fed. Cir. 1995). "When limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention." See Eaton Corp. v. Rockwell Int'l Corp., 66 USPQ2d 1271, 1276 (2003).

Referring to claim 2, the plain language of the body of the claim explicitly refers to and defines the package structure ("power supply voltage node in the package", "being coupled through an internal package node"). When the body of the claim refers to "the package", it is referring back to the particular package previously described in the preamble. Thus, it is clear

that the preamble language referring to the package and the additional references to structural limitations of the package clearly require that "package" be given weight.

Other claims further define the package structure. For example claim 3 recites a multilayered package and that the programmable element is formed of a metallization pattern located on the surface of the package. With respect to claim 3, applicants respectfully submit that MacPherson nowhere teaches a multilayered package and that the programmable element is formed of a metallization pattern located on the surface of the package. Claim 4 recites a multilayered package and that the programmable element is formed of a metallization pattern located on other than the surface of the package. With respect to claim 4, applicants submit that Macpherson fails to teach a multilayered package and that the programmable element is formed of a metallization pattern located on other than the surface of the package. Clearly, such claims are directed towards the package structure and such limitations are not taught by a semiconductor device within a package. Thus, claims 3 and 4 are patentably distinct for these reasons as well.

The Examiner is respectfully requested to reconsider giving patentable weight to the structural limitations of the package described in the claims.

Claims 2, 7-9, 11, 12, 15-18, 20-23, and 27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,536,968 to Crafts et al. The Office Action points to Fig. 3 of Crafts. Fig. 3 is a schematic diagram of a fuse array PROM. (Col 2, lines 61-62). Crafts teaches a programmable read only memory (PROM) including an array of polysilicon fuse elements formed within a semiconductor substrate. See Abstract. Crafts fails to teach a package that includes at least one pair of programmable elements, the one pair including the one one-time programmable element and a second one-time programmable element, the second one-time programmable element having a first and second end, the first end of the second one-time programmable element coupled to a second power supply voltage node and the second end of the second one-time programmable element being coupled through an internal package node to the second end of the first -one-time programmable element as required by claims 2. Even if memory devices are formed in dies in semiconductor packages, as the Examiner suggests, a PROM device and a fuse array structure for implementation within an integrated circuit, as taught by Crafts, fails to teach programmable elements as recited by claim 2. Accordingly,

Applicants respectfully submit that the claim 2 distinguishes over Crafts and respectfully request that the rejection of claim 2 and all claims dependent thereon be reconsidered and withdrawn.

With regards to claim 12, Crafts fails to teach the package comprising at least one one-time programmable element having a first and a second end separated by a programmable link wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package. Craft also completely fails to teach another programmable element serially coupled between the second end of the programmable element and an external package connection. Thus, claim 12 distinguishes over Crafts.

With regards to claim 21, Craft fails to teach a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node and at least one integrated circuit die mounted in the package; and wherein the internal package node couples to an external package connection through another one-time programmable element.

With regards to claim 25, Craft fails to teach a package including one or more one-time programmable elements having a first and a second end separated by a programmable link, wherein the first end of the one one-time programmable element is coupled to a power supply voltage node in the package and a second end of the programmable link is coupled to an internal package node.

In responding to the applicants previous arguments with regards to Crafts, the Office Action, in paragraph 10, argues that Craft teaches a PROM device within a substrate and that a substrate is a package. Applicants respectfully disagree with the Examiner and submit that the semiconductor substrate taught by Crafts is not a package. Craft teaches that the PROM comprises a semiconductor substrate having a first patterned signal layer. (Col. 2, lines 40-43). In no way does Craft's substrate meet the package limitations of the claims at issue.

Claim 12 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,266,829 to Hamdy. The Office Action points to Fig. 5a. Fig. 5a of Hamdy is a circuit

diagram showing an application of the electrically programmable low=impedance anti-fuse of the present invention as a read-only-memory. (Col. 6, lines 32-34). Hamdy teaches that anti-fuses may be formed as a diffusion region in a semiconductor substrate. See Abstract. At col. 3, lines 48-50, Hamdy teaches that "[t]he anti-fuses may be blown either before or after packaging of the integrated circuit die." The semiconductor integrated circuit of Hamdy is distinct from the package. Therefore, Hamdy fails to teach a package for mounting an integrated circuit die comprising at least one one-time programmable element having a first and a second end separated by a programmable link, wherein the first end of the one-time programmable element is coupled to a power supply voltage node in the package and wherein the package further comprises another programmable element serially coupled between the second end of the programmable element and an external package connection.

Claim 12 further recites that another programmable element is serially coupled between the second end of the programmable element and an external package connection. That structure is shown, for example, in Fig. 8 where programmable elements 624-627 are coupled between the second end of programmable element 601-607 and external package connectors. The structure illustrated in Fig. 8 provides, as described on page 10, lines 3-7 of the application, that the fuses 624-627 can be used in testing environments, where, for example, an internal signal must be accessible during test, but is then decoupled from the package pin by blowing a fuse prior to product shipment. That claimed structure and the advantage referenced above is not taught or suggested in any of the references of record alone or in combination.

Hamdy is directed towards electrically programmable interconnect devices for use in integrated circuits. Hamdy fails to teach anything related to one time programmable elements on packages. The Office Action points to elements 168d in Fig. 5a of Hamdy and asserts that element 168h is coupled between a second end of anti-fuse 168d and output 178. According to the Office Action, the first end of anti-fuse 168d is coupled to bit line 00 (the power supply). The Applicants note that the second end of anti-fuse 168d is coupled either to ground through transistor 168d or is floating if the anti-fuse is not programmed. Thus, the element 168h cannot be coupled between the second end as required by the claim and an external package connection. In view of the above remarks, Applicants submit that claim 12 is in condition for allowance.

In paragraph 10, the Examiner responds to the applicants arguments by stating that Hamdy clearly states that the anti-fuses are disposed in an integrated circuit and that the integrated circuit is then packaged. Applicants reiterate that programmable elements inside a semiconductor device do not teach the claimed invention, which is directed to a package. The Examiner further responds to the applicants by referring to col. 13, lines 17-20 of Hamdy where Hamdy point out that when anti-fuse 168 is programmed it is a short circuit. That is exactly the applicants point. When anti-fuse 168 is programmed, it is then connected to ground through the transistor and then element 168h cannot be serially coupled between the second end as required by the claim and an external package connection since the second end is coupled to ground. Otherwise anti-fuse 168 is floating. In neither case is element 168h coupled between the second end of anti-fuse 168 and an external package connection.

Claim 21 stands rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,748,031 to Best. Best teaches fuses in an integrated circuit and fails to teach, as required by claim 21, a package containing one or more one-time programmable elements and an integrated circuit die mounted in the package. Accordingly, Applicants submit that claim 21 distinguishes over Best.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over MacPherson. Applicants submit that claim 6 distinguishes over MacPherson at least for the reasons given for claim 2.

Claims 19 and 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Macpherson further in view of Barth (U.S. Pat. No. 5,134,616). As Applicants explained, MacPherson fails to teach a package including one or more one-time programmable elements as recited in claim 17, on which claims 19 and 24 depend. That teaching is not supplied in Barth. Accordingly, Applicants respectfully request that the rejection of claim 19 and 24 be reconsidered and withdrawn. Further, Barth fails to teach, as recited in claim 19 that the one or more one-time programmable elements specify an operating voltage of at least a portion of a processor. Thus, Applicants respectfully request that the rejection of claim 19 be reconsidered and withdrawn for that additional reason.

Barth and MacPherson, alone or in combination also fail to teach, as recited in claim 24, that the one or more one-time programmable elements specify a control value relating to clock frequency at which the processor operates. Thus, Applicants respectfully request that the rejection of claim 24 be reconsidered and withdrawn for that additional reason.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Macpherson further in view of Barth (U.S. Pat. No. 5,134,616). As Applicants explained, MacPherson fails to teach a package including one or more one-time programmable elements as recited in claim 25. That teaching is not supplied in Barth. Accordingly, Applicants respectfully request that the rejection of claim 25 be reconsidered and withdrawn.

The Office action rejects claim 25 relying on MacPherson and Barth, col. 12, lines 10-34, to teach a semiconductor memory device wherein fuses are programmed to perform an error correction. However, that fails to teach that the claimed programmable element specifies use of ECC for the cache memory on the integrated circuit as claimed in claim 25. Instead Barth teaches using fuses to achieve redundancy by efficiently switching in redundant bit lines. See Summary of the Invention. Barth fails to teach or suggest specifying use of ECC using a programmable element as claimed in claim 25. Accordingly, Applicants respectfully submit that claim 25 distinguishes over the references of record.

In view of the above remarks, Applicants believe that all claims are now in condition for allowance. However, if the Examiner believes there are any issues which could be resolved via a telephone conference, the Examiner is respectfully requested to contact the undersigned at the number indicated below.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Mark Zagorin 7/7/03
Mark Zagorin Date

Respectfully submitted,

Mark Zagorin

Mark Zagorin, Reg. No. 36,0[illegible]
Attorney for Applicant(s)
(512) 347-9030
(512) 347-9031 (fax)

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